

AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A semiconductor apparatus comprising:
 - a semiconductor device;
 - a first dielectric board surrounding the said semiconductor device;
 - a second dielectric board surrounding the said semiconductor device and arranged on the said first dielectric board;
 - a metal cover arranged on the said second dielectric board and above the said semiconductor device;
 - ~~plural~~ external electrodes;
 - upper wiring on said second dielectric board;
 - a first through-hole wiring penetrating the said first dielectric board and electrically connected with the said external electrodes;
 - a second through-hole wiring penetrating the said second dielectric board and electrically connected with the said upper wiring semiconductor device; and
 - an internal wiring ~~inserted~~ between the said first dielectric board and the said second dielectric board₁ ;
 - the wherein said semiconductor device being is connected with the said external electrodes via the said first through-hole wiring, ~~the and said second through-hole wiring and the internal wiring,~~ and ;
 - the wherein said first through-hole wiring and the said second through-hole wiring being are electrically connected with the said internal wiring while being away from each other.
2. (Currently amended) The semiconductor apparatus ~~as claimed in~~ according to claim 1, wherein the said second through-hole wiring is ~~arranged more closely~~ closer to the said semiconductor device than ~~the is said~~ first through-hole wiring is.

3. (Currently amended) The semiconductor apparatus ~~as claimed in~~ according to claim 2, further comprising: wherein

~~a thin metal wire connected to the semiconductor device; and~~

~~an upper wiring arranged on the second dielectric board and connected with the second through-hole wiring;~~

~~the said semiconductor device being is~~ connected to ~~the said~~ upper wiring via ~~the a~~ thin metal wire.

4. (Currently amended) The semiconductor apparatus ~~as claimed in~~ according to claim + 3, further comprising:

a metal plate having ~~the said~~ semiconductor device mounted thereon,

~~the wherein said~~ external electrodes and ~~the said~~ metal plate are co-planar ~~being arranged on the same virtual plane.~~

5. (Currently amended) The semiconductor apparatus ~~as claimed in~~ according to claim + 3, wherein ~~the whole~~ said external electrodes are completely arranged within an outer edge of ~~the said~~ first dielectric board or ~~the said~~ second dielectric board.

6. (Currently amended) The semiconductor apparatus ~~as claimed in~~ according to claim + 3, wherein ~~a part of the~~ said external electrodes is include an external electrode for grounding, and an upper metal layer supplied with a ground potential via ~~the said~~ external electrode for grounding is provided on an upper surface of ~~the said~~ second dielectric board.

7. (Currently amended) The semiconductor apparatus ~~as claimed in~~ according to claim + 3, wherein ~~a part of the~~ said external electrodes is include an external electrode for grounding, and a lower metal layer supplied with a ground potential via ~~the said~~ external electrode for grounding is provided on a lower surface of ~~the said~~ first dielectric board.

8. (New) The semiconductor apparatus according to claim 4, wherein said external electrodes are completely arranged within an outer edge of said first dielectric board or said second dielectric board.

9. (New) The semiconductor apparatus according to claim 4, wherein said external electrodes include an external electrode for grounding, and an upper metal layer supplied with ground potential via said external electrode for grounding is on an upper surface of said second dielectric board.

10. (New) The semiconductor apparatus according to claim 4, wherein said external electrodes include an external electrode for grounding, and a lower metal layer supplied with a ground potential via said external electrode for grounding is on a lower surface of said first dielectric board.

11. (New) The semiconductor apparatus according to claim 1, wherein said semiconductor device is connected to said upper wiring via a thin metal wire.

12. (New) The semiconductor apparatus according to claim 11, further comprising:
a metal plate having said semiconductor device mounted thereon,
wherein said external electrodes and said metal plate are co-planar.

13. (New) The semiconductor apparatus according to claim 11, wherein said external electrodes are completely arranged within an outer edge of said first dielectric board or said second dielectric board.

14. (New) The semiconductor apparatus according to claim 11, wherein said external electrodes include an external electrode for grounding, and an upper metal layer supplied with ground potential via said external electrode for grounding is on an upper surface of said second dielectric board.

15. (New) The semiconductor apparatus according to claim 11, wherein said external electrodes include an external electrode for grounding, and a lower metal layer supplied with a ground potential via said external electrode for grounding is on a lower surface of said first dielectric board.

16. (New) The semiconductor apparatus according to claim 1, further comprising:
a metal plate having said semiconductor device mounted thereon,
wherein said external electrodes and said metal plate are co-planar.

17. (New) The semiconductor apparatus according to claim 1, wherein said external electrodes are completely arranged within an outer edge of said first dielectric board or said second dielectric board.

18. (New) The semiconductor apparatus according to claim 1, wherein said external electrodes include an external electrode for grounding, and an upper metal layer supplied with ground potential via said external electrode for grounding is on an upper surface of said second dielectric board.

19. (New) The semiconductor apparatus according to claim 1, wherein said external electrodes include an external electrode for grounding, and a lower metal layer supplied with a ground potential via said external electrode for grounding is on a lower surface of said first dielectric board.